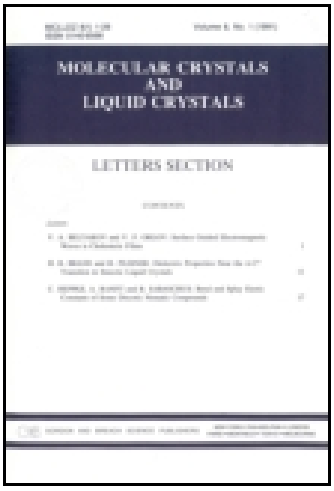

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Effects of Polystyrene Gate Dielectrics with Various Molecular Weights on Electrical Characteristics of Pentacene Thin-Film Transistors

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We report on the molecular weight effect of polystyrene (PS) gate dielectric on the characteristics of pentacene thin-film transistors. Dielectric layers were formed by using three different PS molecules of high molecular weight (PS-H) and low molecular weight (PS-L), and their blend (PS-B). The transistor having the PS-H gate dielectric exhibited the most pronounced drain currents as well as mobility. The gate-leakage current for the device with PS-H was even lower by one order of magnitude than that for the device with PS-L. The results are explained with the relationship between the surface characteristics of gate dielectric layer together with pentacene grain size and the transistor performances.

Keywords Organic transistor; gate dielectric; polystyrene; molecular weight

Introduction

Gate dielectric materials play a key role in improving the performance of organic thin-film transistors (OTFTs) [1]. For example, the gate dielectric layer determines the grain growth and molecular orientation of organic semiconductor in OTFTs. Since the conducting channel in OTFTs is formed in close proximity to the interface between a gate dielectric layer and an organic semiconductor layer, the surface properties of gate dielectric layer in terms of morphological roughness and surface energy must be of primary importance for the device performance [2, 3]. In addition, the leakage current through a gate dielectric layer

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is required to be as low as possible, which is one of significant factors for designing OTFT-based integrated circuits [4]. To date, polymer-based gate dielectric materials have been emerged as a natural component for OTFTs. This is owing to their unique advantages such as mechanical flexibility and low-temperature processability. Therefore, a number of works in this research area have focused on OTFTs with polymeric gate dielectrics. Nevertheless, there are few reports on the effects of molecular weights of polymer gate dielectrics on the characteristics of OTFTs, which are definitely informative for understanding device physics and further advancements of OTFTs.

In this study, we have prepared three different gate dielectric layers using different molecular weights of polystyrene (PS), i.e. Mw 288,000 for high molecular weight PS-H and 45,000 for low molecular weight PS-L and their blend (PS-B) for PS-H:PS-L = 1:1, respectively. Top-contact structured OTFTs are fabricated to investigate the underlying effects of the fabricated gate dielectric layers on the device performance. The surface morphology and surface energy of gate dielectrics are also analyzed with atomic force microscopy (AFM) and contact angle measurements.

Experimental

For the fabrication of OTFTs with top-contact source/drain structure, a glass (Marienfeld 17167) substrate was sequentially cleaned with acetone, iso-propyl alcohol and deionized water. Then, a 150-nm-thick aluminum gate electrode was thermally evaporated onto a glass substrate by using a first shadow mask. Next, different types of PS (Aldrich Co. Ltd), which are PS-H, PS-B, and PS-L, were dissolved into toluene solvent. In order to obtain comparable thickness of a gate dielectric layer, different weight percents for the PS solution (4.3 wt%, 5.4 wt%, 7.0 wt%) were used for PS-H, PS-B and PS-L, respectively. After filtering PS solutions using a 0.45-μm syringe filter, PS dielectric layers were formed by spin-coating and baked for 3 hours at 140°C in dry vacuum oven. Thicknesses of the fabricated gate dielectric layers were almost same as 320 ± 15 nm in each device. Pentacene (TCI Co. LTD) layer, as an organic semiconducting layer, was thermally evaporated through a second shadow mask onto the gate dielectrics with the deposition rate of 0.1 nm/s up to the thickness of 60 nm. Finally, 50-nm-thick gold source and drain electrodes were thermally evaporated using a third shadow mask. The fabricated device configuration is depicted in Fig. 1. During the fabrication processes, all of the vacuum depositions were performed under the base pressure of 1.6×10^{-6} Torr. The channel width and length for the fabricated device are 2000 and 100 μm, respectively.

Electrical characterizations were performed with impedance analyzer (HP 4192LF, Agilent Technologies) and semiconductor analyzer (EL 421C, Elecs Co.). The surface characteristics of films were analyzed with AFM (XE-150, PSIA Inc.) and contact angle measurements.

Results and Discussion

Figure 2 shows the AFM images of the three different gate dielectric layers. The surface morphology together with surface roughness was determined from each AFM data scanned in the area of 5 μm $\times$ 5 μm. As observed in Fig. 2, the PS-H film exhibits the smoothest surface among the three different types of the fabricated films. The average roughness values of the three gate dielectric layers are measured to be about 8.1, 3.4 and 1.9 nm for PS-L, PS-B (i.e. PS_1:1) and PS-H, respectively. Since the PS molecules show relatively hydrophobic nature, it is deduced that higher molecular weight would lead rather smooth

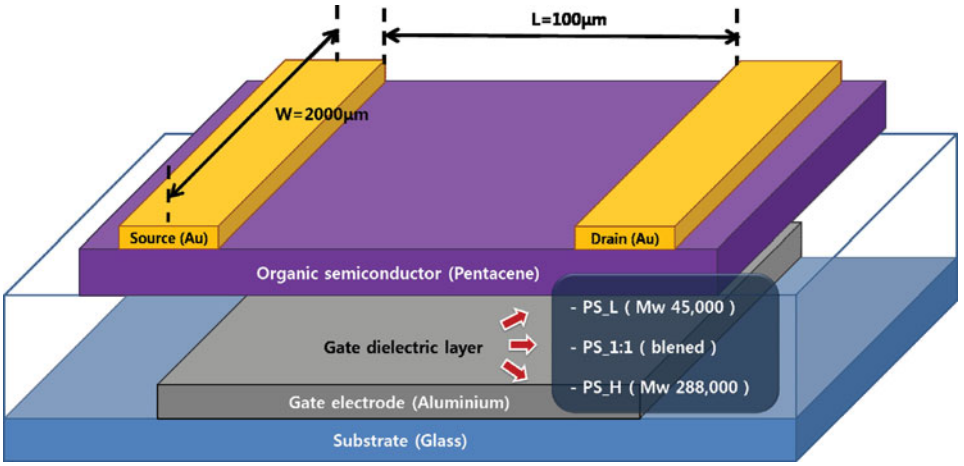

Figure 1. A schematic diagram of a fabricated pentacene TFT with a polymeric insulator having different molecular weight.

surface within the thin-film formation. The fact that polymer chain-ends are closely related to the physical properties of a polymer also implies that the chain ends in the PS-H film might be densely packed, compared to the PS-L case [5]. Further analyses on the packing density of PS chain ends on the film surface are required to elucidate the morphological change arising from different MWs. In addition, this study analyzed the surface energies of the fabricated PS films, which was determined from the magnitude of contact angle. Previously, it was reported that the surface energy of PS films is essentially independent of MW when MW $\geq$ 8,000 [6,7]. Likewise, the magnitude of contact angle of deionized water drop on each surface exhibits almost same as $86 \pm 2^{\circ}$ in our results, as shown in the insets of Fig. 2. Hence, the effect of surface energies would be ignorable.

Figure 3 shows the corresponding AFM images of the 60-nm-thick pentacene layers grown on each gate dielectric layer. The grain size and feature of the pentacene films were determined from each AFM data scanned in the area of 5 μm $\times$ 5 μm. Note that the shape of grain for pentacene films is dendritic, which is in good agreement with previous works employing polymeric insulators for pentacene devices [8]. From Fig. 3, the grain sizes are measured to be about 0.3, 0.5 and 1.0 μm in its diameter for those on PS-L, PS-B (i.e. PS_1:1) and PS-H, respectively. Meanwhile, Choi et al. reported that the morphologies and

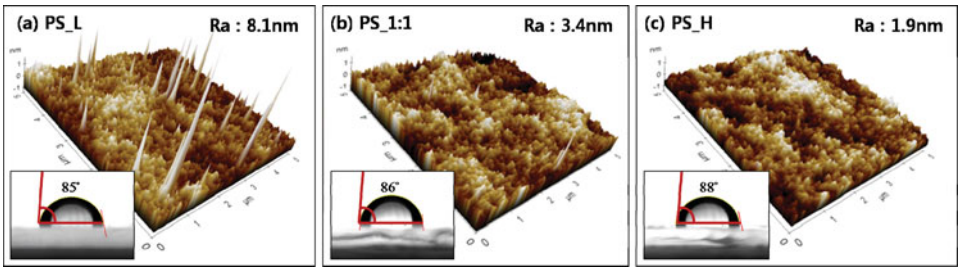

Figure 2. AFM and contact angle images of gate dielectric surface. (a) PS-L, (b) PS-B (i.e. PS_1:1) and (c) PS-H gate dielectric films, respectively. Ra is the abbreviated term of average roughness of gate dielectric surface.

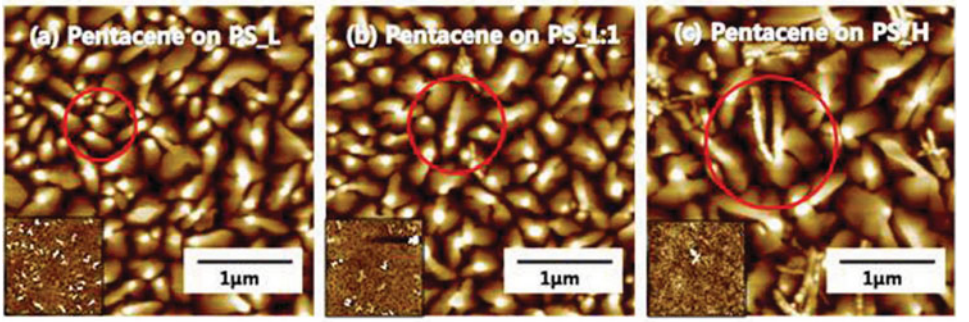

Figure 3. AFM images of 60-nm-thick pentacene layers grown on (a) PS-L, (b) PS-B (i.e. PS_1:1), and (c) PS-H gate dielectric films. The circle indicates the average grain size in each pentacene film. Inset shows the corresponding initial growth of pentacene molecules at the interface.

crystalline ordering of the pentacene films deposited on a PS layer were not significantly varied with the PS MW in the range 8 to 500,000, which could be attributed to similar surface energies of PS films [5]. Although the surface energies of the fabricated PS films were also comparable in our results, the surface roughness was quite different. This result suggests that the smoother surface of gate dielectric layer forms the larger pentacene grains in size. Such an interrelation between the surface roughess of gate dielectric layer and the grain size of the organic semiconductor film is well coincident with many previous works [9, 10]. Interestingly, as shown in inset of Fig. 3, the molecules in a channel regime which induced at the insulator-semiconductor interface within a range of a few nm thick significantly affected by the PS surface according to the molecular weight. With increasing the molecular weight of PS, less void sites were observed at the initial pentacene growth. It results from the smooth surface of PS-H layer. Note that void sites act as a kind of barrier for the charge transport at the channel region during the device operation [11]. Based on the fact that charge transport mainly occurs at the channel region [12], initial pentacene molecular growth together with 60-nm-thick pentacene AFM images would be a good evidence for analyzing the current-voltage characteristics.

The output characteristic curve, drain current (I_D) versus drain voltage (V_D), of the fabricated pentacene TFTs with different gate dielectric layers is shown in Fig. 4(a). Note that the output curve was observed at the gate voltage (V_G) of -40 V. The highest value of the saturation current is observed for the PS-H gate dielectric layer used case. The large drain current results from the large grain size of pentacene molecules induced from less rough surface of PS insulator. Note that higher dielectric capacitance of a gate insulator leads larger drain current at the fixed gate voltage, in other words, higher capacitance can reduce the operating gate voltage for obtaining a required level of drain current. Interestingly, in our results, the highest saturation current for the OTFT with the PS-H type was achieved with even lowest its dielectric capacitance value shown in Fig. 4(b), which is measured from the capacitance-voltage (C-V) characteristics of metal-insulator-semiconductor (MIS) capacitor. Important device properties are extracted from the transfer characteristic plots of $\log_{10}|I_D|-V_G$ and $|I_D|^{1/2}-V_G$ at a negative V_D of -40 V, shown in Fig. 4(c). Among three different types of organic transistors, the highest saturation-region mobility of 0.28 cm^2/Vs for our results was obtained for the device with the PS-H gate dielectric layer. Since the largest pentacene grains grew on the PS-H film, an increase in the mobility can be attributed to less grain boundaries in the pentacene film grown on the

Table 1. The electrical properties of the fabricated three types of pentacene TFTs with different PS dielectric layers

Gate Dielectric	Threshold Voltage (V)	Mobility (cm^2/Vs)	Subthreshold Slope (V/decade)
PS-L	−16	0.18	7.92
PS-B	−16	0.25	4.80
PS-H	−16	0.28	4.22

PS-H gate dielectric layer [13]. Detailed device parameters are summarized in Table 1. Most importantly, the highest leakage currents in the off-state region are observed for the OTFT with the PS-L gate dielectric layer. The inset of Fig. 4(c) also shows conspicuous leakage currents through the gate electrode for the PS-L case. Assuming that the pentacene active layer is totally depleted in the off-stage region under positive V_G, it is possible that more defects generated by ambient molecules might give rise to deep-level traps at the interface between the pentacene and gate dielectric layers so that such traps presumably act as a gate-leakage source. Indeed, ambient molecules such as H_2O and O_2 can permeate

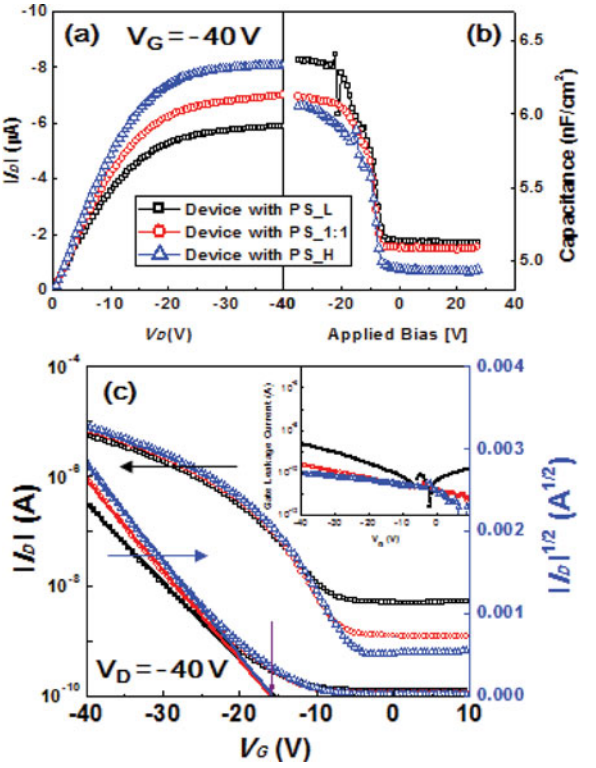

Figure 4. (a) Output characteristics of the fabricated OTFTs and (b) plots of *C-V* characteristics measured with the MIS capacitors according to gate dielectric layers. (c) Transfer characteristics of the fabricated pentacene TFTs. The inset shows the leakage currents−gate voltage curves of the transistors.

easily into the pentacene film having relatively small grains through a large amount of grain boundaries. Although systematic analysis on leakage behavior could not be demonstrated in the present study, it is clearly true that traps are significantly related with gate-leakage exhibitions [14,15]. Consequently, we believe that proper optimization for the molecular weight of polymeric gate-dielectric materials is a prerequisite for the performance of OTFTs.

Conclusion

We investigated the characteristic dependence of pentacene-based OTFTs on the molecular weight of polymeric gate dielectric material. With our firsthand experimentations, large pentacene grains in size and traps induced by interface defects are found to be decisive for the saturation drain current I_D in the on-state and leakage currents in the off-state of OTFTs, respectively. This work demonstrates that a polymeric insulator with higher molecular weight is a promising candidate as an organic-based gate dielectric material for high-performance OTFTs due to low leakage currents as well as high drain currents during device operation, which must be resulted from larger pentacene grains on its smooth surface. Accordingly, we can conclude that the electrical performance of OTFTs is closely related with the molecular weight of polymeric gate dielectric materials. Further studies on other polymeric dielectric materials with various molecular weights still remain to be carried out. This work would provide a scientific platform to build up a high performance showing organic electrical devices.

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